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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/703,181 | 10/30/2000 | Michael T. Moore | CY-0016 | 9600 |

7590 11/17/2004

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| EXAMINER | |
|---|---|
| KIK, PHALLAKA | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/703,181 | MOORE ET AL. | |
| | Examiner | Art Unit | |
| | Phallaka Kik | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action responds to Applicant's amendment filed on 8/19/2003. Claims 1-23 are pending, wherein claims 7-8,21 have been amended.

### *Claim Objections*

2. **Claims 10-11** are objected to because of the following informalities:

As per **claim 10**, "may perform" (lines 2-3) should be --performs-- to clearly identify what is being claimed.

As per **claim 11**, "may" (line 2) should deleted; "may be" (line 4) should be replaced with --are-- to clearly identify what is being claimed.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-20** are rejected under 35 U.S.C. 102(e) as being anticipated by **Miller** (US Patent No. 6,181,164).

As per **claims 1,6-10**, the integrated circuit device with programmable portion (i.e., programmable gate arrays having various arrangements of configurable logic blocks) are described in col. 3, lines 35-45, wherein the communication portion with at least one circuit block manufactured to perform a predetermined data communication function or different functions, including converting received first data values into second data values, correspond to at least the parity generator (col. 4, lines 30-37), Gold code generator (converter of input data words into data words with different values) (col. 8, lines 1-44), and the code scrambler (col. 9, lines 7-32).

As per **claims 2-3**, the programmable portion includes interconnect portion and logic gate portion are inherently part of the configurable blocks and interconnections of the programmable gate array (FPGA) as described in col. 3, lines 35-45 being necessary to implement the method/system on the FPGA, wherein the memory of storing the configuration for the FPGA is also inherently included, being necessary to configure the FPGA to implement the desired functionalities, as is well known in the art.

As per **claim 4**, the timing circuit receiving the clock signal and generating an internal clock with phase shifted with respect to the clock signal is described in col. 8, lines 45-67, wherein since the shift clock-signal is 4 times the clock-chip signal, the shift clock signal is the received clock signal which is phase shifted or delayed to arrive at the slower speed of clock-chip signal (see also col. 6, lines 49-56).

As per **claim 5**, the input/output port is at least described in col. 6, lines 12-32.

As per **claim 11**, the operational control store for providing at least one user operational value configured by a user corresponds to the configuration memory as

discussed in the rejection of claim 3 wherein such user involvement is in the generation of such circuit configuration, which are inherently necessary to implement the method/system on the programmable gate array; and wherein the preset operational values correspond to at least the LUT (look-up table) values as described in col. 5, lines 1-45.

As per **claim 12**, the communication port including multiplexers (MUXes) is also described in col. 5, lines 4-11 and col. 6, lines 12-43.

As per **claim 13**, the compatibility requirement for the data output is also described in col. 6, lines 57-67, as part of the interface with the various standards.

As per **claim 14-17**, the communication portions, selectable or different data communication functions including selectable datapath (i.e., MUXed selectable inputs/outputs) are summarized in col. 2, lines 6-39, wherein the XOR function generator provides for the non-programmable circuits designed to provide a selectable data communication function and the configurable lookup table provides for the selectable data paths (see also Figs. 2-6).

As per **claims 18-20**, the converter (i.e., Gold code generator) and scrambler/de-scrambler are also described in col. 8, lines 1-44 and col. 9, lines 7-32.

5. **Claims 21-23** are rejected under 35 U.S.C. 102(e) as being anticipated by **Killian et al.** (US Patent Application Publication No. 2003/0208723).

As per **claim 21**, the performing of the predetermined function is described in paragraph [0289], and the performing of the serial data communication functions is

described in paragraph [0287] in which the serial port is not synthesized with the logic device configuration data (i.e., serial port is an existing dedicated circuit within the PLD).

As per **claim 23**, the encoding or encryption is also described in paragraph [0012].

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claim 22** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Killian et al.** (US Patent Application Publication No. 2003/0208723) in view of **Miller** (US Patent No. 6,181,164).

As per **claim 22**, **Killian et al.** disclose all of the elements of claim 21, which the claims depend, as discussed in the rejection of claim 21 above, including the scrambling/encryption/encoding function on the serial data communication. However, **Killian et al.** failed to use the polynomial selected for the scrambling/encryption/encoding function. Such use of the polynomial selected for the scrambling/encryption/encoding function is taught in **Miller** (col. 8, lines 1-44; col. 9, lines 7-32). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further include the polynomial selected for the

scrambling/encryption/encoding function as part of the serial communication of **Killian et al.** because such use of polynomial selection allows for better representation and/or selection of the particular bits patterns for scrambling/encryption/encoding as further taught by **Miller et al.** (col. 3, line 62 to col. 4, line 10).

***Remarks***

8. The rejections of claims 1-20 under 35 U.S.C 102(b) as being anticipated by Butts et al. (US Patent No. 5,812,414) are withdrawn in light of Applicant's argument filed on 8/19/2003, wherein as pointed out by Applicant, **Butts et al.**'s conversion is performed by a software tool, instead of the integrated circuit of the system manufactured, as claimed. As given in the new rejection above, **Miller et al.** provides for all of the claimed elements.

9. The rejections of claims 21-23 under 35 U.S.C. 102(b) as being anticipated by **Roush** (US Patent No. 5,457,786) are withdrawn in light of Applicant's arguments filed on 8/19/2003, wherein as pointed out by Applicant, **Roush** does not clearly shows that the step of performing serial data communication functions on a non-synthesized communication portion of the integrated circuit, and further lacks the scrambling/encoding function as claimed. Applicant should note that since the serial communication port used by the PLA is fixed (i.e., non-configurable or already existed in the PLA), it is therefore "non-synthesizable" which is usually the standard found in the communication ports of the programmable logic devices. Applicant should also note that the converting circuit (parallel to serial or serial to parallel) of **Roush** could be construed as scrambling/encoding function. As given in the new rejection above, all

elements of claims 21-23 are taught by **Killian et al.**, and **Killian et al.** in view of **Miller et al.**, respectively.

10. **Claims 10-11** are newly objected to due to the noted informalities as given above.

***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is herein requested to consider them carefully in response to this Office Action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Flexitime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Any response to this action should be mailed to:**

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

**or faxed to:**

703-872-9318 (for Before-Final) and 703-872-9319 (for After-Final) for formal communications intended for entry,

**Or:**

(571) 273-1895 (for informal or draft communications, please label "PROPOSED" or "DRAFT" and let the examiner know prior to faxing).

PK
November 12, 2004

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800